Sworn Declaration to be presented in Patent Prosecution Proceedings

I, the undersigned, Martin Lehnert, having been informed that a false sworn declaration is subject to prosecution as a criminal offence under § 156 of the German Penal Code, hereby make the following sworn deposition which I affirm to be true and accurate to the best of my knowledge.

(1) **An Example Application**

The present invention is operative especially in applications where analog signals are converted into the digital domain by means of A/D converters. Such A/D conversion occurs in many applications in audio and image processing, and in wireless.

One example is a high-speed analog to digital (A/D) converter of limited bitwidth, which is connected to a Digital-Signal-Processor (DSP). This is in accordance with figure *1* of the present application. As shown in that Figure, an 8-bit storage register *1* such as an A/D converter, converts an analog signal of e.g. ± 1V (Volt) to a digital 8-bit 2's complement number. The output bits of the A/D conversion (shown between reference numerals *3* and *4* in the Figure) are connected to the eight most significant bits *5*, of a circuit device e.g. a DSP. Accordingly the least significant bit of the DSP input *6* is set to "1" and the remaining 7 bits of the input bits of the DSP are set to "0".

(2) **Fixed Point Notation**

To illustrate the utility of the present invention, we will refer to normalised fixed-point notation for representing samples.

An A/D converter converts an unlimited number of analog input voltages to a limited number of possible output values. Because, in the example, the output bitwidth of the A/D converter is 8 bits, the A/D converter delivers 2^8 possible codes. In this example, the resolution of the A/D conversion is therefore

[1V-(-1V)]/256 = 2V/256 = 1V/128 = 0.0078125 V per digit.

If the resolution of the A/D conversion is scaled (divided) by the amplitude of the analog input signal the resulting digital number is referred to as being in normalised fixed-point notation. In the example presented in section (1) above, using this normalised fixed-point notation, the 8-bit A/D converter output delivers a fraction of (0.0078125 V) / (1V) = 0.0078125 per digit.

Normalised fixed-point notation is commonly used for signals of limited size. This is the case for A/D converted signals, where the signal is in general limited to a maximum input amplitude and an increase of bitwidth provides a finer resolution of the input signal.

The relation of A/D output in relation to analog input signal is illustrated in the following Table (1):

Analog input signal	A/D converter digital output signal	A/D converter digital output signal in normalised fixed-point notation	A/D converter digital output signal in decimal notation
-1 V	10000000	-1	-128
-0.9921875 V	10000001	-0.9921875	-127
:	:	:	:
-0.0078125 V	11111111	-0.0078125	-1
0 V	00000000	0	0
0.0078125 V	00000001	0.0078125	1
:	:	:	:
≥ 0.9921875 V	01111111	0.9921875	127

Table (1)

(3) **The Examiner's Rejection**

In paragraph 1 of the Examiner's letter, the Examiner gives an example where the binary value 2 of a 4-digit word and the binary value 8 of a 6-digit word yield the same result after expansion. The inherent assumption, which the Examiner makes from classical integer number theory, is that for the initial numbers the least significant bit represents the value $2^0=1$, the next higher bit represents $2^1= 2$ and so on. It is correct that under this assumption it is not possible to perform a useful addition.

However, the expansion due to the invention is applicable, where the **Most Significant Bit** of each of both input is taken to represent the same value. This assumption is common practice for engineers working with signal amplitude levels within a limited range such as those involved with A/D Convertors, where an increase in bitwidth corresponds to a finer resolution of the signal. More generally, it is an assumption common in applications of radar, imaging, wireless and measuring equipment. Such an assumption is made when, for example, one analog input signal of ±1V is converted by a 4-digit and a 6-digit A/D-converter, and then the resulting values are added. This situation is shown in the following Figure (A).

Considering the case shown in Figure (A), the digital output numbers of the A/D-converters have different resolution, namely 0.125 for the 4-bit A/D-converter (4-digit word 0010), and 0.03125 for the 6-bit A/D-converter (6-digit word 001000).
Direct binary addition of both numbers would give the expected result of 0.5.

If both input data are expanded to 16 bit numbers according to the method described in the present invention and added, the result would be: (0010000000000001) + (0010000000000001) = (0100000000000010).

This corresponds to 0.50006103515625 in normalised fixed-point notation explained above. Thus the deviation from the mathematically correct value of 0.5 is 0.00006103515625. Taking into account the resolution of the input words, given by the resolution of 0.125 for the 4-digits word, and 0.03125 for the 6-digit word, the error introduced by the invention is

negligible in most applications. (The error is typically much smaller than the signal noise introduced by the resolution of the A/D conversion.)

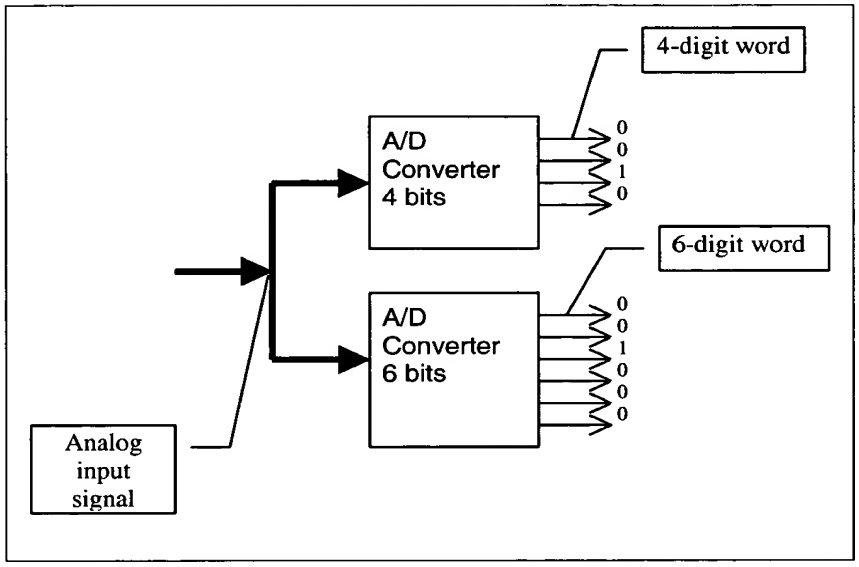

Figure (A)

The following Table (2) shows how analog input values are converted into digital numbers. The representation in normalised fixed-point notation (see (2) above) and the representation in integer format are also included for ease of comparison. Note especially the row for analog input signal 0.25V.

Analog input signal	4-bit A/D converter digital output signal	4-bit A/D converter digital output signal in decimal notation	6-bit A/D converter digital output signal	6-bit A/D converter digital output signal in decimal notation	A/D converter digital output signal in normalised fixed-point notation
-1 V	1000	-8	100000	-32	-1
-0.96875 V			100001	-31	-0.96875
-0.93750 V			100010	-30	-0.93750
-0.90625 V			100011	-29	-0.90625
-0.875 V	1001	-7	100100	-28	-0.875
-0.84375 V			100101	-27	-0.84375
-0.81250 V			100110	-26	-0.81250
-0.78125 V			100111	-25	-0.78125
-0.75 V	1010	-6	101000	-24	-0.75
:	:	:	:	:	:
:	:	:	:	:	:
-0.125 V	1111	-1	111100	-4	-0.125
-0.09375 V			111101	-3	-0.09375
-0.06250 V			111110	-2	-0.06250
-0.03125 V			111111	-1	-0.03125
0 V	0000	0	000000	0	
0.03125 V			000001	1	0.03125
0.06250 V			000010	2	0.06250
0.09375 V			000011	3	0.09375
0.125 V	0001	1	000100	4	0.125
0.15625 V			000001	5	0.15625
0.18750 V			000010	6	0.18750
0.21875 V			000011	7	0.21875
0.25 V	0010	2	001000	8	0.25
:	:	:	:	:	:
:	:	:	:	:	:
0.875 V	0111	7	011100	28	0.875
0.90625 V			011101	29	0.90625
0.93750 V			011110	30	0.93750
0.96875 V			011111	31	0.96875

Table (2)

In Table (2), as previously mentioned, the Most Significant Bits of 2 words of different size are taken to be equivalent. Thus in the given example the binary value 2 in a 4-digit word (0010) is equivalent to the binary value 8 in a 6-digit word (001000), which is equivalent to 0.25 in normalised fixed-point notation.

(4) More about the Example Application

As mentioned in section (1) in one example application the values are input to a digital signal processor (DSP). The DSP applies a digital filter algorithm to the received input words to reduce input noise and to extract the required component of the input signal. The filter algorithm consists of multiplications of the input data with given coefficients, stored inside the DSP. It is assumed that the coefficients also have a resolution of 8 bits and are located in the most significant bits positions of the available 16 bits to allow for maximum precision. Thus all possible coefficients occupy, in normalised fixed-point notation, the range from –1 up to 0.9921875.

The worst case happens for multiplication of the minimum A/D converted value with the minimum coefficient. (In Table (2) it can be seen that for normalised fixed-point notation the value"+1" is not allowed. The multiplication would cause an overflow and a wrong result. To avoid wrong results, an additional check for overflow is added to the filter calculations inside the DSP.)

Considering the example application of the invention described in section (1) above, the minimum input value for the DSP is binary (1000000000000001), corresponding to -0.999969482421875 in normalised fixed-point notation. A multiplication of the minimum DSP input value with the minimum coefficient therefore yields -0.999969482421875 * -1 = 0.999969482421875. This result corresponds to binary (0111111111111111), which is the maximum positive value. The modification by the invention corresponds to the addition of 1/32768 = 0.000030517578125 in normalised fixed-point notation. This error can be tolerated, because it is much smaller than the signal noise introduced by the A/D conversion.

(5) Applicability to other systems

The invention is also applicable to other systems than the particular example described above. The A/D conversion may have various signal amplitudes. Instead of an A/D converter and DSP, the eight bit storage register *1* and circuit device *8* shown in figure *1* of the present application may consist of multiplexers, registers, shift registers or other dedicated hardware.

Furthermore, the position of the added "1" bit may be different from the least significant bit *6* shown in figure 1 of the present application. The bitwidth of from storage register *1* and circuit device 8 may be different from the example values of 8 bits and 16 bits.

(6) Summary

It has been shown that there are examples where the invention can be used. A particular example has been explained in detail. Furthermore it has been shown how potential errors relative to a mathematically correct result that are introduced by the invention are negligible in practical applications. Accordingly, utility of the invention has been shown.

I hereby declare and affirm that the foregoing statement is true and accurate to the best of my knowledge.

Nuremberg, Date: May 5th 2004

Martin Lehnert

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